AMENDMENTS TO THE CLAIMS

1. (Original) An MRAM cell, comprising:

a pinned magnetic layer having an interior region and a peripheral region;

a sense magnetic layer having an interior region and a peripheral region respectively aligned with the interior region and peripheral region of the pinned layer;

a tunnel junction layer having an interior region and a peripheral region, and provided between and aligned with the interior regions and the peripheral regions of the pinned and sense magnetic layers; and

a first spacer layer formed between the peripheral regions of the tunnel junction layer and the peripheral region of at least one of the pinned and sense magnetic layers.

2. (Original) The MRAM cell according to claim 1, wherein the first spacer layer is composed of an insulator material.

3. (Original) The MRAM cell according to claim 2, wherein the first spacer layer is composed of a material selected from the group consisting of silicon dioxide, silicon nitride, and silicon carbide.

4. (Original) The MRAM cell according to claim 3, wherein the first spacer layer is composed of silicon dioxide.

5. (Original) The MRAM cell according to claim 1, wherein the first spacer layer has a thickness of 700-1000 Angstroms.

6. (Original) The MRAM cell according to claim 1, wherein the pinned magnetic layer comprises:

a first magnetic layer having an interior region and a peripheral region;

an antiferromagnetic layer having an interior region and a peripheral region aligned with the interior region and the peripheral region of the first magnetic layer;

a second magnetic layer having an interior region and a peripheral region aligned with the interior regions and the peripheral regions of the first magnetic layer and the antiferromagnetic layer; and

a second spacer layer formed between the peripheral region of the antiferromagnetic layer and the peripheral region of one of the first and second magnetic layers.

7. (Original) The MRAM cell according to claim 6, wherein the first and second spacer layers are each composed of an insulator material.

8. (Original) The MRAM cell according to claim 7, wherein the first and second spacer layers are each composed of a material selected from the group consisting of silicon dioxide, silicon nitride, and silicon carbide.

9. (Original) The MRAM cell according to claim 8, wherein at least one of the first and second spacer layers is composed of silicon dioxide.

10. (Original) The MRAM cell according to claim 6, wherein the first and second spacer layers each has a thickness of 700-1000 Angstroms and the first and second magnetic layers each have a thickness of 10-100 Angstroms.

11. (Original) The MRAM cell according to claim 1, further comprising:

a conductive layer having an interior region and a peripheral region aligned with the interior regions and the peripheral regions of the pinned and sense magnetic layers, wherein the interior region of the conductive layer is adjacent to the interior region of one of the pinned and sense magnetic layers; and

a second spacer layer formed between the peripheral region of the conductive layer and the peripheral region of the adjacent pinned or sense magnetic layer.

12. (Original) The MRAM cell according to claim 11, wherein the first and second spacer layers are each composed of an insulator material.

13. (Original) The MRAM cell according to claim 12, wherein the first and second spacer layers are each composed of a material selected from the group consisting of silicon dioxide, silicon nitride, and silicon carbide.

14. (Original) The MRAM cell according to claim 13, wherein at least one of the first and second spacer layer is composed of silicon dioxide.

15. (Currently Amended) The MRAM cell according to claim 11, wherein the first and second spacer layers each has a thickness of 700-1000 Angstroms and the sense magnetic layer has a thickness of 10-100 Angstroms.

16. (Currently Amended) The MRAM cell according to claim 11, wherein the pinned magnetic layer ~~element~~ comprises:

a magnetic seed layer having an interior region and a peripheral region;

an antiferromagnetic layer having an interior region and a peripheral region;

a ferromagnetic layer having its magnetic orientation pinned by the antiferromagnetic layer, an interior region and a peripheral region; and

a third spacer layer formed between the peripheral region of the antiferromagnetic layer and the peripheral region of one of the magnetic seed layer and ferromagnetic layer.

17. (Original) The MRAM cell according to claim 16, wherein the first, second and third spacer layers are each composed of an insulator material.

18. (Currently Amended) The MRAM cell according to claim ~~12~~17, wherein the first, second and third spacer layers are each composed of a material selected from the group consisting of silicon dioxide, silicon nitride, and silicon carbide.

19. (Currently Amended) The MRAM cell according to claim ~~13~~18, wherein at least one of the first, second and third spacer layers is composed of silicon dioxide.

20. (Currently Amended) The MRAM cell according to claim ~~11~~16, wherein the first, second and third spacer layers each has a thickness of 700-1000 Angstroms and the

~~first, second and third magnetic layer~~ antiferromagnetic and ferromagnetic layers each have ~~has~~ a thickness of 10-100 Angstroms.

21. (Original) A multilayer memory cell stack, comprising:

a first conductive layer having a circumferential edge region;

a second conductive layer having a circumferential edge region; and

a spacer layer made of an insulator material and provided between the respective circumferential edge regions of the first and second conductive layers such that the first and second conductive layers are more closely spaced to each other at regions thereof other than at the respective circumferential edge regions.

22. (Original) The multilayer memory cell stack according to claim 21, wherein the memory cell stack is an MRAM cell.

23. (Original) The multilayer memory cell stack according to claim 21, wherein the memory cell stack is a PCRAM cell.

24. (Original) The multilayer memory cell stack according to claim 21, wherein the spacer layer is composed of a material selected from the group consisting of silicon dioxide, silicon nitride, and silicon carbide.

25. (Original) The multilayer memory cell stack according to claim 24, wherein the spacer layer is composed of silicon dioxide.

26. (Currently Amended) The multilayer memory cell stack according to claim ~~25~~21, wherein the spacer layer has a thickness of 700-1000 Angstroms and the first and second conductive layers each have a thickness of 10-100 Angstroms.

27.-53. (Canceled).

54. (Original) A processing system, comprising:

a processor for receiving and processing image data;

an MRAM memory device comprising a plurality of MRAM cells for exchanging data with said processor; and

a memory controller for managing memory access requests from the processor to the at least one memory device,

wherein each MRAM cell comprises:

a pinned magnetic layer having an interior region and a peripheral region;

a sense magnetic layer having an interior region and a peripheral region respectively aligned with the interior region and peripheral region of the pinned layer;

a tunnel junction layer having an interior region and a peripheral region, and provided between and aligned with the interior regions and the peripheral regions of the pinned and sense magnetic layers; and

a first spacer layer formed between the peripheral regions of the tunnel junction layer and the peripheral region of at least one of the pinned and sense magnetic layers.

55. (Original) The processor according to claim 54, wherein the pinned magnetic layer of each MRAM cell comprises:

a first magnetic layer having an interior region and a peripheral region;

an antiferromagnetic layer having an interior region and a peripheral region;

a second magnetic layer having an interior region and a peripheral region; and

a second spacer layer formed between the peripheral region of the antiferromagnetic layer and the peripheral region of one of the first and second magnetic layers.

56. (Original) The processor according to claim 54, wherein each MRAM cell further comprises:

a conductive layer having an interior region and a peripheral region aligned with the interior regions and the peripheral regions of the pinned and sense magnetic layers, wherein the interior region of the conductive layer is adjacent to the interior region of one of the pinned and sense magnetic layers; and

a second spacer layer formed between the peripheral region of the conductive layer and the peripheral region of the adjacent pinned or sense magnetic layer.